Amendments to the Specification:

Please replace paragraph [0011] on page 3 bridging page 4 with the following amended paragraph.

[0011] Besides, this invention also provides a manufacturing method for said semiconductor package. The manufacturing method mainly comprises the following steps. Firstly, a substrate array comprising two substrate units is provided. Therein, the substrate unit has an upper surface, a lower surface and a cutting street formed on the upper surface and connecting two substrate units. Moreover, there are a plurality of through holes formed at the cutting street and passing through the upper surface and the lower surface. Next, said substrate array is singulated along the cutting street so as to separate said substrate units into two individual substrate units, wherein each individual substrate unit has a side surface, and to separate the through holes into a plurality of ~~recessions~~ recesses formed at one side surface of each individual substrate unit. Then, a chip is provided to dispose on one of said individual substrate units and electrically connected to said individual substrate unit via a plurality of bumps. Finally, a plurality of electrically conductive devices, for example solder balls, are mounted to the ~~recessions~~ recesses. Thus, said semiconductor package is formed according to the steps as shown above.

On page 5 bridging page 6, please replace paragraph [0023] with the following amended paragraph.

[0023] In accordance with the preferred embodiment as shown in FIGs. 3, 4, 5 and 6, there is provided a semiconductor package. The semiconductor package mainly comprises a substrate unit 31 and a chip 32. The substrate unit 31 has an upper surface 311, an opposite lower surface 312 and a side surface 313 connecting the upper surface 311 and the lower surface 312. Therein, there are a plurality of circuit traces 314

formed on the upper surface 311, and there are a plurality of ~~recessions~~ recesses 315, for example slots as shown in FIG. 5, formed on the side surface [[315]]313, wherein each ~~recessions~~ recesses 315 has a metal layer formed thereon. The ~~recessions~~ recesses 315 are electrically connected to the circuit traces 314. As mentioned above, the metal layer can be a copper layer, a nickel layer and a gold layer formed on the ~~recessions~~ recesses 315 in sequence. As shown in FIG. 6, the chip 32 has an active surface 321 with a plurality bonding pads 323 formed thereon, and an opposite back surface 322. Therein, a plurality of bumps 324 are formed on the bonding pads 323 as shown in FIG. 3. In addition, the active surface 321 of the chip 32 faces the upper surface 311 of the substrate 31 and is disposed thereon via the bumps 324 for electrically connecting the chip 32 to the substrate 31. Therein, the chip 32 is made of a material of silicon; the bumps 324 are formed on the bonding pads 323 by the method of plating or screen-printing a solder material on the bonding pads 323 and then performing a reflow process.

On page 6, please replace paragraphs [0025] and [0026] which bridges page 7 with the following amended paragraphs.

[0025] Moreover, a plurality of electrically conductive devices are mounted to the ~~recessions~~ recesses 315 of the side surface 313 to electrically connect the substrate 31 and external devices, for example a package module substrate and a motherboard. Thus the signal of the chip 32 can be transmitted to external electronic devices through the substrate 31 and said electrically conductive devices. Because the recesses 315 of the side surface 313 of the substrate 31 are connected to electrically conductive devices, the ~~recessions~~ recesses 315 can be regarded as contacts and replaces substrate pads formed on a lower surface of a conventional substrate.

[0026] Next, ~~pay attention~~ please refer to FIG. 7 to specify the forming method of the ~~recessions~~ recesses 315. Firstly, a substrate array 34 is provided. Therein, the

substrate array 34 comprises two substrate units 31. And the substrate array 34 has an upper surface 311, a lower surface 312 and a cutting street 316 formed between the substrate units 31. Furthermore, there are a plurality of through holes 317 formed at the cutting street 316 and passing through the upper surface 311 and the lower surface 312. The through holes 317 can be formed by the methods of mechanical drilling, laser ablation, photochemical reaction and plasma etching. Afterwards, the substrate array 34 is singulated into two individual substrate units 31 as shown in FIG. 4 so that the through holes 317 are separated into a plurality of ~~recessions~~ recesses 315 formed on the side surface 313 of each individual substrate unit 31. In addition, the inner walls of the through holes 317 are plated with metal layers before the substrate array 34 is singulated. Therein, the process of plating a metal layer on the inner wall of one of the through holes 317 comprises plating a copper layer on the inner wall of the through hole 317. Because the inner wall of the through hole 317 is made of a non-conductive material, said a material for activation, for example barium, is disposed on the inner wall in advance. Then a thin copper layer is formed on said material for activation by electro-less plating, wherein the thickness of the thin copper layer is about 0.5 um. Next, a thicker copper layer is formed on said thin copper layer, wherein the thickness of the thicker copper layer is about 20 um. In addition, the copper layer can be formed by the method of direct plating. The process of direct plating comprises the following steps. Firstly, a conductive polymer layer is formed on the inner wall of the through hole 317. Next, a metal layer is formed on the conductive polymer layer by the method of plating. As mentioned, when the copper layer is plated on the inner wall of the through hole, a nickel layer and a gold layer are plated in sequence on the copper layer. Thus, the ~~recessions~~ recesses 315 can be regarded as contacts for electrically connecting to external electronic devices.

On page 8, please replace paragraph [0027] with the following amended paragraph.

[0027] Moreover, said semiconductor package as mentioned above can be electrically connected to another electronic devices, for example another semiconductor package with the same type, via a plurality of electrically conductive devices. Accordingly, said semiconductor package can be electrically connected to the same one to form a package module. Referring to FIG. 8, a semiconductor package module comprises two semiconductor packages 4, a plurality of electrically connecting devices 43, for example solder balls, and a module substrate 6. Therein, the semiconductor packages 4 are the same as mentioned above. Each semiconductor package 4 mainly comprises an upper surface 411, an opposite lower surface 412 and a side surface 413 connecting the upper surface 411 and the lower surface 412. There are a plurality of ~~recessions~~ recesses 414 formed on the side surface 414. And a plurality of electrically connecting devices 43, for example solder balls, are formed on the ~~recessions~~ recesses 414 so as to electrically connect to the module substrate 6. Moreover, the chip 42 is bonded to the substrate 41 in a flip chip manner. Then, said semiconductor packages are attached to each other by attaching a lower surface 412 of on substrate unit 41 in one package to a back surface 421 of one chip 42 in another package via an adhesive layer 5 as shown in FIG. 8.